Attorney Docket No.: 062986.0174

Serial No.: 09/788,174

Inventor: Kenneth C. Yeager, et al. Art Unit: 2113

Confirmation No.: 4017

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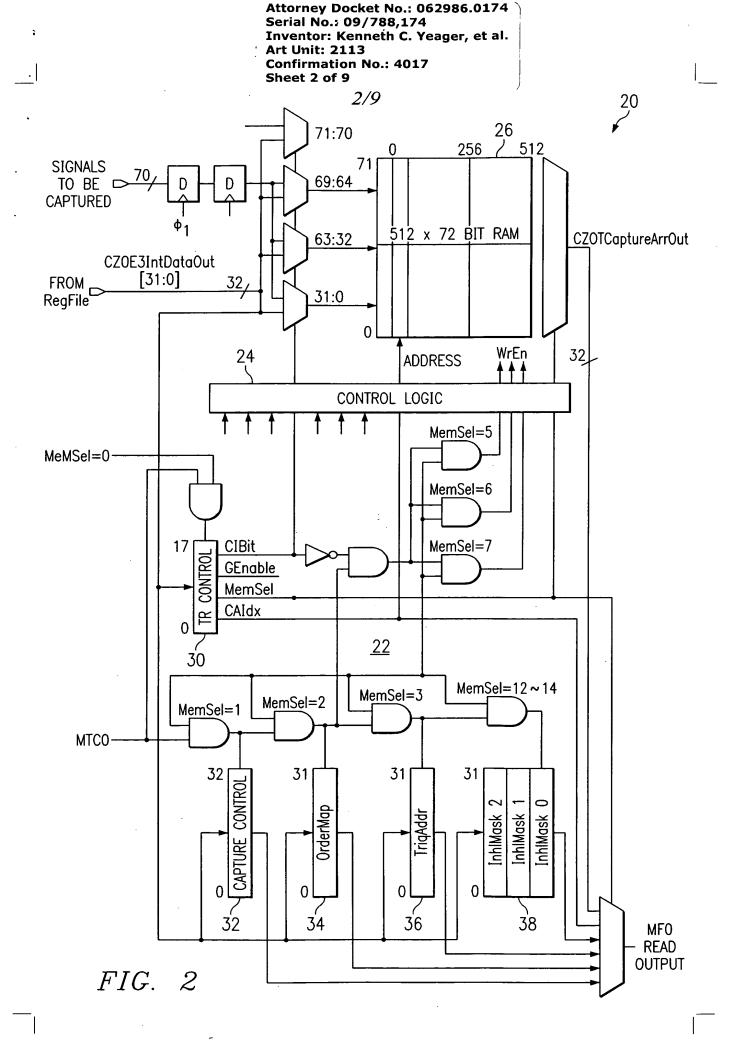
1/9



10

'N1' CHIP CPU IQ INT 22 24 20--12 FQ FLT PT PC MAP **TRIGGER** CONTROLLER AQ **PROGRAM** TRACE **RECORDER INVISIBLE** INSTRUCTION 512 x 72-BIT DATA CACHE SIGNALS -CACHE INSIDE CHIP RAM 26 16 14 **SYSTEM** SECONDARY CACHE INTERFACE 17 18 LOGIC ANALYZER -28 **ETC VISIBLE** SYSTEM **EXTERNAL SIGNALS** 29 CACHE BUS

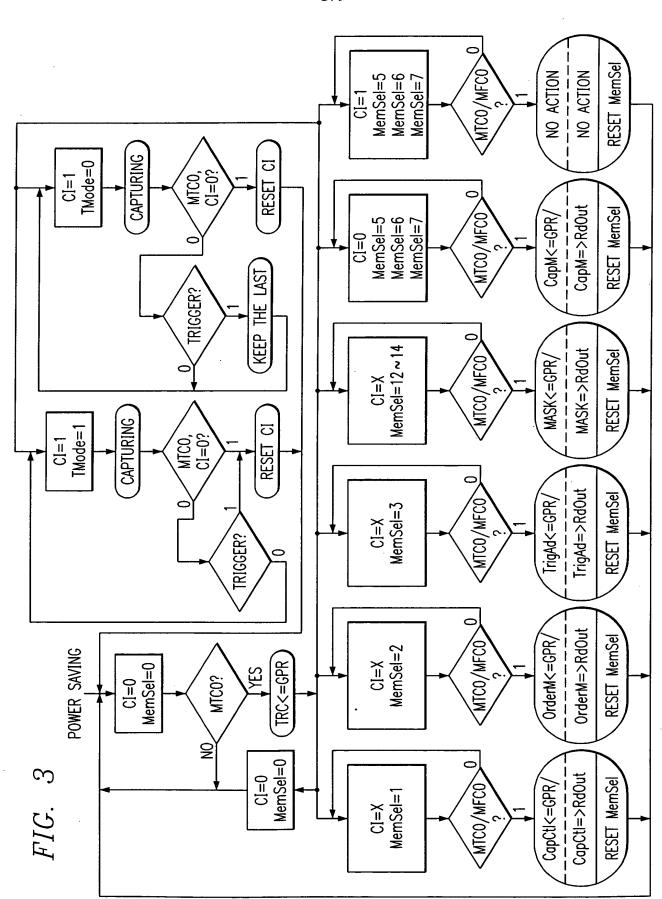
FIG. 1



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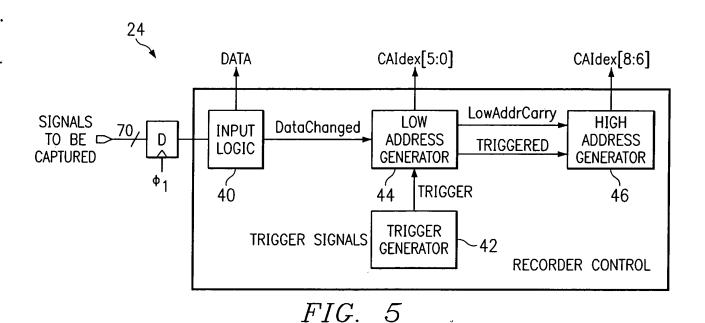
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NThEventMode
NoChangeAll
NThCycleMode
NoChangeAll
NoChangeAll
NoChangeAll
NThCycleMode
NThCycleMode
NThCycleMode
NThCycleMode

FIG. 6

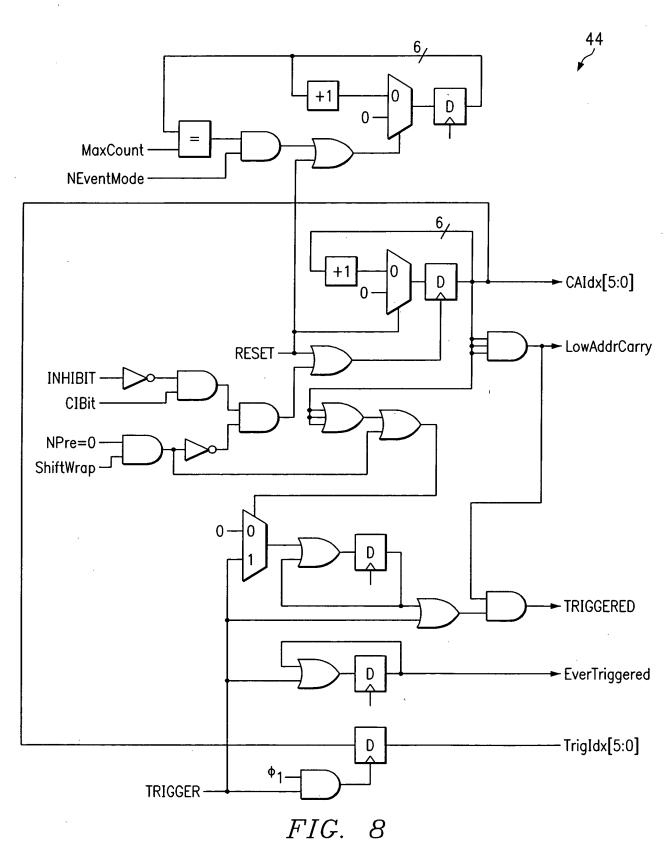
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Sheet 6 of 9 6/9 TrigAddr[2] TrigAddr[31] TrigAddr[30] TrigAddr[4] TrigAddr[3] MuxOut[31] MuxOut[30] MuxOut[4] MuxOut[3] MuxOut[2] DecSel TrigAddr[1]-IVA[1] TrigAddr[0] IVA[31:2] HighMatch IVA[0] Decoded[3] Decoded[2] LowMatch Decoded[1] Decoded[0] TrigAddr[1] **IVAMatch** IVA[1] TrigAddr[0] IVA[0]-SkipN IntervalTrigger Count<N Count<N Inh CZ2WtchTrigger □ TriggerMask Trigger GRADUATES □ GR0TAGradOr CpuHang D **RESET** FIG. 7 NCycleTrigger TrigCntReset

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Attorney Docket No.: 062986.0174 Serial No.: 09/788,174 Inventor: Kenneth C. Yeager, et al. Art Unit: 2113 Confirmation No.: 4017 Sheet 8 of 9 8/9 PRELOAD NPost NPre FIG. 9 +1 NBlock CntReset CntEqN **TRIGGER BLOCKO** ShiftWrap NPreEq0 INITIALIZE -LowAddrCarry CAIdx[8:6]-ShiftWrap NPre=7 NPre=6 NPre=5 NPre=4 NPre=3 NPre=2

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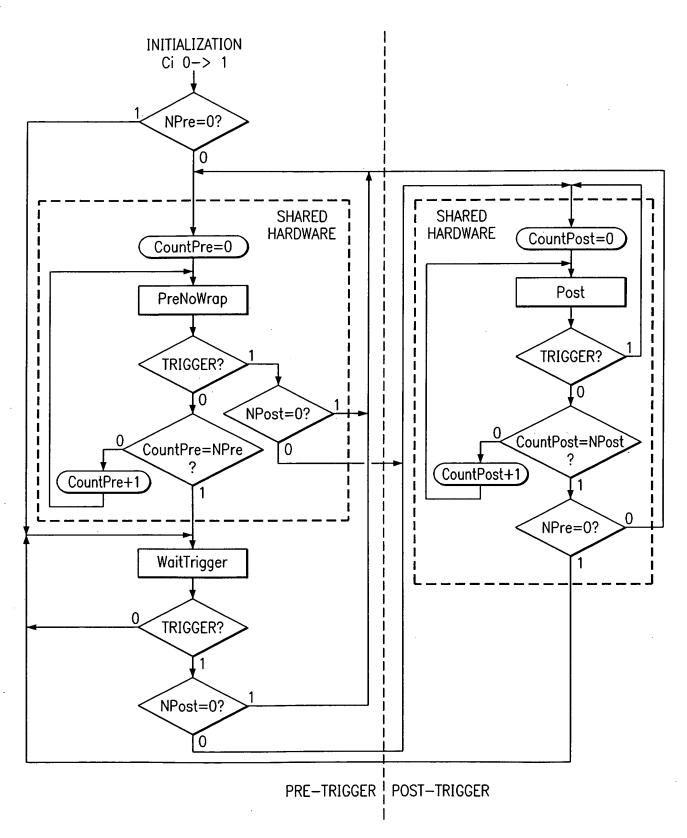


FIG. 10